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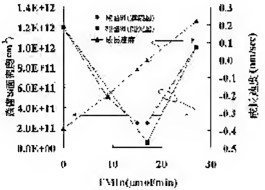
(54) METHOD OF CLEANING AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method of removing contamination due to impurities and physical damages onto the surface of a semiconductor substrate before crystal growth or on the surface of a semiconductor before regrowth, with a minimum change in shape, without inducing the diffusion of impurities or crystal defects in an original semiconductor layer.

SOLUTION: In a crystal growth apparatus, a material having etching action and a material for crystal growth are supplied at the same time onto the surface of a semiconductor wafer to be well-balanced between an etching rate and a crystal growth speed, resulting in the efficient removal of residual impurities.



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[Claim(s)]

[Claim 1]A pure disposal method which removes a contaminant adhering to the surface of a semiconductor layer, comprising:
An etching nature substance which has an etching operation to said semiconductor layer.
A pure processing process which makes crystal growth materials contact said semiconductor layer by turns simultaneous.

[Claim 2]A pure disposal method including a pure processing process of exposing the surface of said semiconductor layer in atmosphere containing an etching nature substance which is a pure disposal method which removes a contaminant adhering on the surface of a semiconductor layer, and has an etching operation to said semiconductor layer, and crystal growth materials.

[Claim 3]It is a pure disposal method which removes a contaminant adhering on the surface of a semiconductor layer, A pure disposal method including a pure processing process of supplying simultaneously the first gas containing an etching nature substance which has an etching operation to said semiconductor layer, and the second gas containing crystal growth materials to the surface of said semiconductor layer.

[Claim 4]A pure disposal method characterizing by supplying intermittently said first gas and said second gas in the pure disposal method according to claim 3.

[Claim 5]A pure disposal method, wherein a difference of layer thickness of said semiconductor layer before and after carrying out said pure processing process in the pure disposal method according to any one of claims 1 to 4 is 100 nm or less.

[Claim 6]A pure disposal method characterized by keeping layer thickness of said semiconductor layer from decreasing substantially in the pure disposal method according to any one of claims 1 to 5 when carrying out said pure processing process.

[Claim 7]A pure disposal method controlling layer thickness change of said semiconductor layer in the pure disposal method according to claim 5 or 6 by adjusting a quantity ratio of said etching nature substance and said crystal growth materials.
[Claim 8]In the pure disposal method according to claim 3 or 4, [numerals of layer thickness variation speed of said semiconductor layer] Layer thickness variation speed of said semiconductor layer at the time of defining a case where positive and layer thickness decrease a case where layer thickness increases as negative, and carrying out said pure processing process R, Layer thickness variation speed of said semiconductor layer at the time of supplying only said first gas to said semiconductor layer surface r_1, When layer thickness variation speed of said semiconductor layer at the time of supplying only said second gas to said semiconductor layer surface is made into r_2, -- a pure disposal method characterized by adjusting the amount of supply of said first gas and said second gas so that an absolute value of layer thickness variation speed of these may become $|R|<|r_2|<|r_1|$.
[Claim 9]A pure disposal method characterized by being $R< 0$ in the pure disposal method according to claim 8.
[Claim 10]A pure disposal method characterized by $|R|$ being 0.1nm/sec or less in the pure disposal method according to claim 8 or 9.
[Claim 11]A pure disposal method, wherein said crystal growth materials contain an element which constitutes said semiconductor layer in the pure disposal method according to any one of claims 1 to 10.
[Claim 12]A pure disposal method, wherein said crystal growth materials contain an organic metal in the pure disposal method according to any one of claims 1 to 11.
[Claim 13]A pure disposal method characterized by said etching nature substance being a halogen element or its compound in the pure disposal method according to any one of claims 1 to 12.
[Claim 14]A pure disposal method, wherein said semiconductor layer consists of compound semiconductors in the pure disposal method according to any one of claims 1 to 13.
[Claim 15]A pure disposal method, wherein said semiconductor layer consists of an III-V fellows compound semiconductor in the pure disposal method according to claim 14.
[Claim 16]A pure disposal method characterized by said crystal growth materials being the compounds containing an III fellows element which constitutes said semiconductor layer in the pure disposal method according to claim 15.
[Claim 17]A pure disposal method, wherein an III fellows element which constitutes said semiconductor layer consists of one kind in the pure disposal method according to claim 15 or 16.
[Claim 18]A pure disposal method, wherein an III fellows element which constitutes said

semiconductor layer in the pure disposal method according to any one of claims 15 to 17 is indium (In).
[Claim 19]A manufacturing method of a semiconductor device characterized by comprising the following.
A process of forming the first semiconductor layer in the upper part of a semiconductor substrate.
A process of carrying out pure processing of the surface of said first semiconductor layer.
An etching nature substance in which said process of carrying out pure processing of the surface of said first semiconductor layer has an etching operation to said semiconductor layer including a process of forming the second semiconductor layer on said first semiconductor layer.
A process which makes crystal growth materials contact the surface of said semiconductor layer.

[Claim 20]A process of forming the first semiconductor layer in the upper part of a semiconductor substrate, and a process of carrying out pure processing of the surface of said first semiconductor layer, [including a process of forming the second semiconductor layer on said first semiconductor layer] [said process of carrying out pure processing of the surface of said first semiconductor layer] A manufacturing method of a semiconductor device including a process of exposing the surface of said semiconductor layer in atmosphere containing an etching nature substance which has an etching operation to said semiconductor layer, and crystal growth materials.
[Claim 21]A manufacturing method of a semiconductor device including a process of supplying simultaneously the first gas and the second gas containing crystal growth materials characterized by comprising the following to the surface of said semiconductor layer.
A process of forming the first semiconductor layer in the upper part of a semiconductor substrate.
A process of carrying out pure processing of the surface of said first semiconductor layer.
An etching nature substance in which said process of carrying out pure processing of the surface of said first semiconductor layer has an etching operation to said semiconductor layer including a process of forming the second semiconductor layer on said first semiconductor layer.

[Claim 22]A manufacturing method of a semiconductor device characterizing by supplying intermittently said first gas and said second gas in a manufacturing method of the semiconductor device according to claim 21.
[Claim 23]A manufacturing method of a semiconductor device with which a difference of layer

thickness of said first semiconductor layer before and after carrying out said process of carrying out pure processing of the surface of said first semiconductor layer, in a manufacturing method of the semiconductor device according to any one of claims 19 to 22 is characterized by being 100 nm or less.
[Claim 24]A manufacturing method of a semiconductor device characterized by keeping layer thickness of said first semiconductor layer from decreasing substantially when carrying out said process of carrying out pure processing of the surface of said first semiconductor layer, in a manufacturing method of the semiconductor device according to any one of claims 19 to 23.
[Claim 25]A manufacturing method of a semiconductor device controlling layer thickness change of said first semiconductor layer in a manufacturing method of the semiconductor device according to claim 23 or 24 by adjusting a quantity ratio of said etching nature substance and said crystal growth materials.
[Claim 26]In a manufacturing method of the semiconductor device according to claim 21 or 22, [numerals of layer thickness variation speed of said first semiconductor layer] Layer thickness variation speed of said first semiconductor layer at the time of carrying out said process of defining a case where positive and layer thickness decrease a case where layer thickness increases as negative, and carrying out pure processing of the surface of said first semiconductor layer R, Layer thickness variation speed of said first semiconductor layer at the time of supplying only said first gas to said first semiconductor layer surface r_1, When layer thickness variation speed of said first semiconductor layer at the time of supplying only said second gas to said first semiconductor layer surface is made into r_2, -- a manufacturing method of a semiconductor device characterized by adjusting the amount of supply of said first gas and said second gas so that an absolute value of layer thickness variation speed of these may become $|R|<|r_2|<|r_1|$.
[Claim 27]A manufacturing method of a semiconductor device characterized by being $R< 0$ in a manufacturing method of the semiconductor device according to claim 26.
[Claim 28]A manufacturing method of a semiconductor device characterized by $|R|$ being 0.1nm/sec or less in a manufacturing method of the semiconductor device according to claim 26 or 27.
[Claim 29]A manufacturing method of a semiconductor device, wherein said crystal growth materials contain an element which constitutes said first semiconductor layer in a manufacturing method of the semiconductor device according to any one of claims 19 to 28.
[Claim 30]A manufacturing method of a semiconductor device, wherein said crystal growth materials contain an organic metal in a manufacturing method of the semiconductor device according to any one of claims 19 to 29.
[Claim 31]A manufacturing method of a semiconductor device characterized by said etching

nature substance being a halogen element or its compound in a manufacturing method of the semiconductor device according to any one of claims 19 to 30.

[Claim 32]A manufacturing method of a semiconductor device, wherein said first semiconductor layer consists of compound semiconductors in a manufacturing method of the semiconductor device according to any one of claims 19 to 31.

[Claim 33]A manufacturing method of a semiconductor device, wherein said first semiconductor layer consists of an III-V fellows compound semiconductor in a manufacturing method of the semiconductor device according to claim 32.

[Claim 34]A manufacturing method of a semiconductor device being a compound in which said crystal growth materials contain an III fellows element which constitutes said semiconductor layer in a manufacturing method of the semiconductor device according to claim 33.

[Claim 35]A manufacturing method of a semiconductor device, wherein an III fellows element which constitutes said semiconductor layer consists of one kind in a manufacturing method of the semiconductor device according to claim 34.

[Claim 36]A manufacturing method of a semiconductor device, wherein an III fellows element which constitutes said semiconductor layer in a manufacturing method of the semiconductor device according to claim 35 is indium (In).

[Claim 37]A manufacturing method of a semiconductor device forming said first semiconductor layer and said second semiconductor layer with vapor phase epitaxy in a manufacturing method of the semiconductor device according to any one of claims 19 to 36.

[Claim 38]In a manufacturing method of the semiconductor device according to any one of claims 19 to 37, A manufacturing method of a semiconductor device carrying out said process of carrying out pure processing of the surface of said first semiconductor layer after forming a mask on said first semiconductor layer after a process of forming said first semiconductor layer, and removing said mask continuously.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the art which cleans the semiconductor layer surface.

[0002]

[Description of the Prior Art]In the manufacturing process of a semiconductor device, the crystal growth process of the semiconductor layer of the same kind or of a different kind to a semiconductor substrate top, The re-growth process of a semiconductor layer of the same kind or of a different kind [for the patterning process by the photo lithography, chemical etching, or

dry etching which used the dielectric etc. as the mask, and a current block structure or optical confinement structure] is repeated in many cases. In this case, if the substrate face in front of crystal growth and the semiconductor growth layer surface before re-growth tend to receive impurities contamination and a physical damage according to processes, such as air exposure, etching, washing, and crystal growth is performed on those surfaces as it is, the element characteristic and a life will deteriorate sharply. For this reason, in order to remove impurities contamination and a physical damage layer, it etched in the crystal growth interior of a room, and the technique of performing crystal growth continuously has been used after that.
[0003]As such art, [the patent No. 3158651] [by using trimethylgallium (TMG) and Al Singh (AsH_3) as growth materials, using hydrogen chloride (HCl) as etching gas, and etching in the growth interior of a room just before re-growth of GaAs] If impurities, such as carbon (C), oxygen (O), and silicon (Si), can be removed and TMG is simultaneously supplied with HCl during etching, the gap from the SUTOIKIOME tree produced on the crystal surface by etching is compensated, and it is supposed that accumulation of the carrier in a re-growth interface will be controlled.
[0004]JP,S59-65434,A has disclosed the art which introduces simultaneously steam of the alkyl compound of an III fellows element and hydroxide of V fellows element, or an alkyl compound, and etches a semiconductor layer with hydrogen chloride in the vapor phase epitaxy of a GaAs semiconductor. As for the speed of etching, the example with an etching rate of 0.1 micrometer/m is shown. By carrying out like this, it is supposed that the Shimoji surface before a growth start can be made into a specular surface.
[0005]To JP,S51-74580,A, gaseous phase etching of the semiconductor substance which comprises an III-V fellows element is carried out under the inactive gas atmosphere containing the halogenation thing and the hydroxide of V fellows element, and the art which introduces hydroxide of V fellows element simultaneously is indicated to it. According to the gazette, it is indicated that it is flat and the substrate face excellent in specular surface nature can be obtained.
[0006]
[Problem to be solved by the invention]However, in the above-mentioned conventional technology, a contaminant with a slow etching rate remains easily on the surface compared with the composing element of a semiconductor crystal, For example, IEEE jar NARUOBU Selected . Topics Inn KANTAMU Electronics . The 3rd volume As reported to the 853rd (IEEE Journalof Selected Topics in Quantum Electronics, Vol.3, N0.3, p845-p853) page from of 3 No. the 845th page, Using PCl_3 as etching gas, even if it etches the InP surface in the growth interior of a room, most Si(s) will not be etched but will remain on the surface. Near [usual in this invention persons' experimental result] crystal growth temperature, even if it gave etching in the crystal growth interior of a room as shown by the patent No. 3158651, it was not easy to

remove the remains Si of a re-growth interface. When it etched too much deeply by removing the remains Si, raising substrate temperature too much and being sufficient, impurity diffusion and a crystal defect were produced inside the semiconductor layer of a basis, or shape change occurred by etching, and there was a problem that the device structure as a design was unproducible.

[0007][a place which this invention is made in light of the above-mentioned circumstances, and is made into the purpose] It is in making shape change into the minimum and providing the technique of removing stably impurities contamination and a physical damage on the semiconductor substrate surface in front of crystal growth, or the surface of a semiconductor before re-growth with sufficient reproducibility, without inducing impurity diffusion in a semiconductor layer of a basis, and generating of a crystal defect.

[0008]

[Means for solving problem]About a Reason with difficult removal of a specific contaminant adhering to the semiconductor surface, this invention persons guessed as follows. When an etching nature substance is made to act to a contaminant adhering to the semiconductor layer surface, an etching nature substance and the above-mentioned specific contaminant start a chemical reaction. However, even if associative strength of combination produced by this chemical reaction is comparatively weak, and a contaminant combines with an etching nature substance, forms a compound and is desorbed from the semiconductor surface, it is expected that combination goes out immediately and it re-adheres to the semiconductor surface. Thus, since a specific contaminant adhering to the semiconductor surface re-adheres to a semiconductor layer, removal is imagined to be difficult.

[0009]By making both materials with an etching operation, and crystal growth materials contact the semiconductor layer surface used as a candidate for pure processing, a basis of a such guess and this invention person found out that the etching removal of the contaminant could be carried out efficiently, controlling re-adhesion, and completed this invention.

[0010]The etching nature substance which is a pure disposal method which removes the contaminant adhering on the surface of the semiconductor layer according to this invention, and has an etching operation to said semiconductor layer, A pure disposal method including the pure processing process which makes crystal growth materials contact said semiconductor layer by turns simultaneous is provided.

[0011]According to this invention, it is a pure disposal method which removes the contaminant adhering on the surface of the semiconductor layer, A pure disposal method including the pure processing process of exposing the surface of said semiconductor layer in the atmosphere containing the etching nature substance which has an etching operation to said semiconductor layer, and crystal growth materials is provided.

[0012]According to this invention, it is a pure disposal method which removes the contaminant

adhering on the surface of the semiconductor layer, A pure disposal method including the pure processing process of supplying simultaneously the first gas containing the etching nature substance which has an etching operation to said semiconductor layer, and the second gas containing crystal growth materials to the surface of said semiconductor layer is provided.
[0013]If an etching nature substance acts on the semiconductor layer surface, the contaminant adhering to the semiconductor layer surface will be desorbed from the surface. However, a part of the contaminant from which it was desorbed may adhere to the semiconductor layer surface again. In order to raise the cleanliness factor of a semiconductor layer, it is necessary to fully control re-adhesion of such a contaminant. So, in this invention, an etching nature substance and crystal growth materials are contacted on the semiconductor layer surface, and etching removal of the contaminant is carried out efficiently, controlling re-adhesion. Although the Reason for the ability to prevent re-adhesion of a contaminant with such a technique is not necessarily clear, after a contaminant is desorbed from the semiconductor layer surface, it is imagined as what is depended on the site which the contaminant occupied till then being promptly occupied with crystal growth materials.
[0014]In the pure disposal method of this invention, said first gas and said second gas can have composition supplied intermittently. By carrying out like this, contamination of the surface of a semiconductor layer can be removed much more efficiently.
[0015]In the pure disposal method of this invention, the difference of the layer thickness of said semiconductor layer before and after carrying out said pure processing process can have composition which is 100 nm or less. By carrying out like this, a cleanliness factor high enough is realizable.
[0016]In the pure disposal method of this invention, when carrying out said pure processing process, the layer thickness of said semiconductor layer can have composition kept from decreasing substantially. Here, even if the layer thickness of said semiconductor layer does not decrease at all or "it does not decrease substantially" has reduction of some layer thickness, the layer thickness variation speed says that it is 0.1nm/sec or less. With constituting so that the layer thickness of said semiconductor layer may not decrease substantially, a cleanliness factor high enough is realizable about the semiconductor layer surface.
[0017]As mentioned above, a cleanliness factor high enough is realizable by controlling layer thickness change of the semiconductor layer which is the target of pure processing. Although this Reason is not necessarily clear, after a contaminant is desorbed from the semiconductor layer surface, it is imagined as what is depended on the site which the contaminant occupied till then certainly being occupied with crystal growth materials. The control can adjust the quantity ratio of an etching nature substance and said crystal growth materials for layer thickness change of said such semiconductor layer, for example. For example, the

semiconductor layer used as the candidate for pure processing is not etched substantially, and a new semiconductor layer can be prevented from growing up to be the upper part of the semiconductor layer concerned substantially by adjusting appropriately the quantity ratio of etching nature gas and material gas, and supplying the semiconductor layer surface. Re-adhesion of an etching nature substance and the substance etched when the balance with crystal growth materials collapsed and having been inclined to the etching side arises, and sufficient cleanliness factor may not be obtained. On the other hand, when it inclines to the direction of membrane formation, while a contaminant is not fully removed by it, a new semiconductor layer laminates, and sufficient cleanliness factor is not obtained.

[0018]In the pure disposal method of this invention, [the numerals of the layer thickness variation speed of said semiconductor layer] The layer thickness variation speed of said semiconductor layer at the time of defining the case where positive and layer thickness decrease the case where layer thickness increases as negative, and carrying out said pure processing process R, The layer thickness variation speed of said semiconductor layer at the time of supplying only said first gas to said semiconductor layer surface r_1, When layer thickness variation speed of said semiconductor layer at the time of supplying only said second gas to said semiconductor layer surface is made into r_2, The absolute value of such layer thickness variation speed can have composition which adjusts the amount of supply of said first gas and said second gas so that it may become $|R|<|r_2|<|r_1|$.

[0019]By carrying out like this, the supply balance of an etching nature substance and crystal growth materials becomes suitable, and while the contaminant adhering to the semiconductor layer surface is removed efficiently, re-adhesion in the semiconductor layer of the contaminant from which it was desorbed can be controlled.

[0020]In the pure disposal method of this invention, it can have composition which is $R< 0$. By carrying out like this, a cleanliness factor high enough is realizable about the semiconductor layer surface.

[0021]In the pure disposal method of this invention, $|R|$ can have composition which is 0.1nm/sec or less. By carrying out like this, the supply balance of an etching nature substance and crystal growth materials becomes still more suitable, and while the contaminant adhering to the semiconductor layer surface is removed efficiently, re-adhesion in the semiconductor layer of the contaminant from which it was desorbed can be controlled. It becomes easy [the design of element structure].

[0022]In the pure disposal method of this invention, said crystal growth materials can have composition containing an organic metal.

[0023]In the pure disposal method of this invention, said etching nature substance can have composition which is a halogen element or its compound.

[0024]In the pure disposal method of this invention, it can have composition which said semiconductor layer becomes from a compound semiconductor.
[0025]Said semiconductor layer shall consist of an III-V fellows compound semiconductor in the pure disposal method of this invention.
[0026]When it is considered as the compound containing the III fellows element which constitutes said semiconductor layer for crystal growth materials, the composing element of the semiconductor layer concerned can be made to occupy the empty lattice position in the semiconductor layer formed with the etching nature substance, and strange stratification etc. can be prevented from forming in the surface.
[0027]The III fellows element which constitutes said semiconductor layer shall consist of one kind. By carrying out like this, it can suppress that formation of strange stratification and composition change take place during the pure processing on the surface of a semiconductor layer.
[0028]In the pure disposal method of this invention, the III fellows element which constitutes said semiconductor layer can have composition which is indium (In). In the vapor phase epitaxy of InP, the growth temperature of 600 to 650 ** is usually adopted. This is for preventing diffusion of impurities, such as zinc, and obtaining the impurities profile as a design, for example, it was added intentionally, in order to give conductivity to a crystal, while preventing the phosphorus which is V fellows element from ****ing. However, such when a low-temperature growth temperature is adopted comparatively, pure processing of a growth interface becomes much more difficult. Generally, removal efficiency becomes high, so that pure processing of the growth interface by etching nature gas makes ambient temperature high temperature. However, in an InP semiconductor system, since a maximum exists in pure treatment temperature, contamination of a growth interface is hard to be removed and especially contamination of silicon poses a serious problem. According to this invention, the problem of contamination of this growth interface is effectively solvable.
[0029]According to this invention, a manufacturing method of a semiconductor device shown below is provided. Here, with a semiconductor device, electronic devices, such as optical elements, such as a light emitting element, a photo acceptance unit, and an optical modulator, a field effect transistor, a bipolar transistor, are included.
[0030]A process of forming the first semiconductor layer in the upper part of a semiconductor substrate according to this invention, [including a process of carrying out pure processing of the surface of said first semiconductor layer, and a process of forming the second semiconductor layer on said first semiconductor layer] [said process of carrying out pure processing of the surface of said first semiconductor layer] A manufacturing method of a semiconductor device including a process which makes an etching nature substance which has an etching operation to said semiconductor layer, and crystal growth materials contact the

surface of said semiconductor layer is provided.

[0031]A process of forming the first semiconductor layer in the upper part of a semiconductor substrate according to this invention, [including a process of carrying out pure processing of the surface of said first semiconductor layer, and a process of forming the second semiconductor layer on said first semiconductor layer] [said process of carrying out pure processing of the surface of said first semiconductor layer] A manufacturing method of a semiconductor device including a process of exposing the surface of said semiconductor layer in atmosphere containing an etching nature substance which has an etching operation to said semiconductor layer, and crystal growth materials is provided.

[0032]The process of forming the first semiconductor layer in the upper part of a semiconductor substrate according to this invention, [including the process of carrying out pure processing of the surface of said first semiconductor layer, and the process of forming the second semiconductor layer on said first semiconductor layer] [said process of carrying out pure processing of the surface of said first semiconductor layer] The manufacturing method of a semiconductor device including the process of supplying simultaneously the first gas containing the etching nature substance which has an etching operation to said semiconductor layer, and the second gas containing crystal growth materials to the surface of said semiconductor layer is provided.

[0033]If an etching nature substance acts on the semiconductor layer surface, the contaminant adhering to the semiconductor layer surface will be desorbed from the surface. However, a part of the contaminant from which it was desorbed may adhere to the semiconductor layer surface again. In order to raise the cleanliness factor of a semiconductor layer, it is necessary to fully control re-adhesion of such a contaminant. So, in this invention, an etching nature substance and crystal growth materials are contacted on the semiconductor layer surface, and etching removal of the contaminant is carried out efficiently, controlling re-adhesion. Although the Reason for the ability to prevent re-adhesion of a contaminant with such a technique is not necessarily clear, after a contaminant is desorbed from the semiconductor layer surface, it is imagined as what is depended on the site which the contaminant occupied till then being promptly occupied with crystal growth materials.

[0034]In the manufacturing method of the semiconductor device of this invention, said first gas and said second gas can have composition supplied intermittently. By carrying out like this, contamination of the surface of a semiconductor layer can be removed much more efficiently.

[0035]In the manufacturing method of the semiconductor device of this invention, the difference of the layer thickness of said first semiconductor layer before and after carrying out said process of carrying out pure processing of the surface of said first semiconductor layer can have composition which is 100 nm or less. By carrying out like this, a cleanliness factor high enough is realizable.

[0036]In the manufacturing method of the semiconductor device of this invention, when carrying out said process of carrying out pure processing of the surface of said first semiconductor layer, the layer thickness of said first semiconductor layer can have composition kept from decreasing substantially. Here, even if the layer thickness of the first semiconductor layer does not decrease at all or "it does not decrease substantially" has reduction of some layer thickness, the layer thickness variation speed says that it is 0.1nm/sec or less. With constituting so that the layer thickness of the first semiconductor layer may not decrease substantially, a cleanliness factor high enough is realizable about the semiconductor layer surface.

[0037]As mentioned above, a cleanliness factor high enough is realizable by controlling layer thickness change of the first semiconductor layer that is the target of pure processing. Although this Reason is not necessarily clear, after a contaminant is desorbed from the semiconductor layer surface, it is imagined as what is depended on the site which the contaminant occupied till then certainly being occupied with crystal growth materials. The control can adjust the quantity ratio of an etching nature substance and said crystal growth materials for layer thickness change of such first semiconductor layer, for example. For example, the semiconductor layer used as the candidate for pure processing is not etched substantially, and a new semiconductor layer can be prevented from growing up to be the upper part of the semiconductor layer concerned substantially by adjusting appropriately the quantity ratio of etching nature gas and material gas, and supplying the semiconductor layer surface. Re-adhesion of an etching nature substance and the substance etched when the balance with crystal growth materials collapsed and having been inclined to the etching side arises, and sufficient cleanliness factor may not be obtained. On the other hand, when it inclines to the direction of membrane formation, while a contaminant is not fully removed by it, a new semiconductor layer laminates, and sufficient cleanliness factor is not obtained.

[0038]In a manufacturing method of a semiconductor device of this invention, [numerals of layer thickness variation speed of said first semiconductor layer] Layer thickness variation speed of said first semiconductor layer at the time of carrying out said process of defining a case where positive and layer thickness decrease a case where layer thickness increases as negative, and carrying out pure processing of the surface of said first semiconductor layer R, Layer thickness variation speed of said first semiconductor layer at the time of supplying only said first gas to said first semiconductor layer surface r_1, When layer thickness variation speed of said first semiconductor layer at the time of supplying only said second gas to said first semiconductor layer surface is made into r_2, -- an absolute value of layer thickness variation speed of these can have composition which adjusts the amount of supply of said first gas and said second gas so that it may become $|R|<|r_2|<|r_1|$. By carrying out like this, supply balance of

an etching nature substance and crystal growth materials becomes still more suitable, and while a contaminant adhering to the semiconductor layer surface is removed efficiently, re-adhesion in a semiconductor layer of a contaminant from which it was desorbed can be controlled.

[0039]In a manufacturing method of a semiconductor device of this invention, it can have composition which is R< 0. By carrying out like this, a cleanliness factor high enough is realizable about the semiconductor layer surface.

[0040]In the manufacturing method of the semiconductor device of this invention, |R| can have composition which is 0.1nm/sec or less. By carrying out like this, the supply balance of an etching nature substance and crystal growth materials becomes still more suitable, and while the contaminant adhering to the semiconductor layer surface is removed efficiently, re-adhesion in the semiconductor layer of the contaminant from which it was desorbed can be controlled.

[0041]In the manufacturing method of the semiconductor device of this invention, said crystal growth materials can have composition containing an organic metal.

[0042]In the manufacturing method of the semiconductor device of this invention, said etching nature substance can have composition which is a halogen element or its compound.

[0043]In the manufacturing method of the semiconductor device of this invention, it can have composition which said first semiconductor layer becomes from a compound semiconductor.

[0044]The first semiconductor layer shall consist of an III-V fellows compound semiconductor in the manufacturing method of the semiconductor device of this invention. At this time, account crystal growth materials can have composition which is a compound containing the III fellows element which constitutes the first semiconductor layer. The III fellows element which constitutes the first semiconductor layer shall consist of one kind. By carrying out like this, it can suppress that formation of strange stratification and composition change take place during the pure processing on the surface of a semiconductor layer.

[0045]In the manufacturing method of the semiconductor device of this invention, the III fellows element which constitutes the first semiconductor layer can have composition which is indium (In). In the vapor phase epitaxy of InP, the growth temperature of 600 to 650 ** is usually adopted. This is for preventing diffusion of the zinc of impurities, while preventing the phosphorus which is V fellows element from ****ing, and obtaining the impurities profile as a design. However, such when a low-temperature growth temperature is adopted comparatively, pure processing of a growth interface becomes much more difficult. Generally, removal efficiency becomes high, so that pure processing of the growth interface by etching nature gas makes ambient temperature high temperature. However, in an InP semiconductor system, since a maximum exists in pure treatment temperature, contamination of a growth interface is hard to be removed and especially contamination of silicon poses a serious problem.

According to this invention, the problem of contamination of the starting growth interface is effectively solvable.
[0046]In the manufacturing method of the semiconductor device of this invention, it can have composition which forms said first semiconductor layer and said second semiconductor layer with vapor phase epitaxy.
[0047]In the manufacturing method of the semiconductor device of this invention, after the process of forming said first semiconductor layer, a mask is formed on said first semiconductor layer, and after removing said mask continuously, it can have composition which carries out said process of carrying out pure processing of the surface of said first semiconductor layer. When it passes through such a process, the first semiconductor layer surface turns into the re-growth surface, and many impurities adhere to the surface easily by survival of contamination by the atmosphere, and mask material, etc. According to this invention, such impurities are efficiently removable.
[0048]
[Mode for carrying out the invention][a semiconductor layer which is the target of pure processing in this invention] InP systems, such as InGaAs, InGaAsP, AlGaInAs, and InAsP, GaAs systems, such as AlGaAs, InGaP, AlGaInP, GaAsSb, and InGaAsN, III-V fellows compound semiconductor;ZnSe(s), such as GaN systems, such as GaN, AlGaN, GaInN, AlGaInN, and BAlGaInN, It is constituted by semiconductors, such as the compound, germanium, silicon, and its compound besides compound semiconductors, such as II-VI fellows compound semiconductor [, such as ZnTe, MgZnSSe, MgZnCdSe, MgZnSeTe, ZnSeTe, ZnO, MgZnO, and MgCdZnO,];. A 3 yuan system or composition more than 4 former system may be sufficient as a semiconductor layer which is the target of pure processing in this invention.
[0049]Among these, a prominent effect is acquired when this invention is applied to removal of a contaminant which adhered to the surface of an III-V fellows compound semiconductor layer by the production processes or air exposure of an element. It is especially effective if fully removing especially depending on conventional technology applies to removal of difficult silicon.
[0050]A halogen element or its compound which combines with a large majority of elements, and forms a volatile compound as an etching nature substance in this invention can be illustrated. Among these, it is preferably used at a point that handling is easy that they are materials containing chlorine (Cl).
[0051]As an etching nature substance in this invention, t-butyl chloride (CH_3) $(_3CCl$:TBCl), Bisdimethyl amino phosphine chloride $([(CH_3)\ _2]\ N_2PCl$:BDMAPCl), Hydrogen chloride (HCl), and chlorination methyl $(CH_3\ Cl)$, a carbon tetrachloride (CCl_4), bisdimethyl amino ARUSHIN

chloride ([$(CH_3)_2$] N_2AsCl), phosphorus trichloride (PCl_3), 3 chlorination arsenic $AsCl_3$, chlorine (Cl_2), and same Br system materials and I system -- materials and F system -- materials can be illustrated. Among these, if t-butyl chloride is used, it can etch effectively, maintaining SUTOIKIMETORI of a semiconductor layer which is the target of pure processing comparatively good. For example, if a semiconductor layer which is the target of pure processing contains V fellows element of a different kind from what is contained in etching gas when the above-mentioned semiconductor layer contains V fellows element with specific etching gas with an III-V fellows semiconductor, Although a problem by which a denaturation layer will be formed on the surface during pure processing often arises, since t-butyl chloride does not contain V fellows element, a denaturation layer is not formed during pure processing and it is preferred. Since the temperature dependence of etching capability is comparatively controlled when bisdimethyl amino phosphine chloride is used, stable pure processing can be performed.

[0052]When the III fellows element which constitutes the semiconductor layer which is the target of pure processing consists of one kind, The III fellows element which is desirable since it is hard to cause formation of strange stratification and composition change during the surface treatment of this invention, and also constitutes the first semiconductor, [indium (In)] for example, InP, InAs, InN, InSb, etc. come out, or gallium (Ga), for example, GaAs, GaP, GaN, GaSb, etc. come out, and, in a certain case, a more prominent effect shows up.

[0053]When this invention carries out growth of a semiconductor layer using a vapor phase growth system, a prominent effect is acquired and the more prominent effect in the case of the organic metal vapor-phase-epitaxy (MOCVD:Metal Organic Vapor Phase Epitaxy) method for having used the organic metal for growth materials shows up. About the hydrogen compound and organic metal gas which are crystal growth materials, limitation in particular is not carried out in this case, but what is necessary is just to use a hydrogen compound and organometallic compound gas required to obtain a desired compound semiconductor.

[0054]

[Working example]Although the embodiment of this invention is explained in full detail below, referring to the attached Drawings that the above and other purposes, the feature, and advantage of this invention should be made clear, this invention is not limited to an embodiment, unless the gist is exceeded.

[0055]The first embodiment this example explains remains impurities removal of the growth interface in the case of re-growing up InP on InP using the MOVPE method. Trimethylindium (TMIn) and phosphine (PH_3) were used as crystal growth materials, using t-butyl chloride (CH_3) ($_3$CCl:TBCl) as materials which have an etching operation. After growing up 1.0 micrometer of undoping InP layers 103 as 1st growth layer by the decompression (60Torr)

MOVPE method on the Sn dope {001} InP board 101 like drawing 1, a wafer is once taken out from a MOVPE furnace and air exposure is carried out for 12 hours. Wet processing is not carried out. Then, this wafer was again thrown in in the MOVPE furnace, and the 0.5-micrometer undoping InP layer 105 was growth re-grown up as 2nd growth layer.

[0056]By the second growth interface 104 in front of the 2nd growth start, TBCl, TMIn, and PH_3 were supplied for 10 minutes on the surface of the wafer in the MOVPE furnace, and surface pure processing was performed (sample A). The amount of supply of TBCl in the case of this surface pure processing is 19.4micromol/min, This is made into the etching rate of InP and corresponds 20.5 nm/min, and the amount of supply of 15.08micromol/min and PH_3 of the amount of supply of TMIn is 2.68 mmol/min, and these are made into the growth rate of InP, and are equivalent to 20.5 nm/min. Therefore, the etching rate of InP by TBCl and the growth rate of InP by TMIn and PH_3 are equal, and there is no layer thickness change of the undoping InP layer 103 which grew up into the 1st time during this surface pure processing. The substrate temperature at the time of surface pure processing was 625 **.

[0057]The sample (sample B) which started growth of the 2nd undoping InP layer 105 without performing surface pure processing by the second TBCl, TMIn, and PH_3 in the growth interface 104 in front of the 2nd InP layer growth start for comparison was also produced.

[0058]The depth direction was analyzed carrying out sputtering of the undoping InP layer 105 using a secondary ion mass analysis method (SIMS) about the remains impurity density in the re-growth interface of two samples, the sample A and the sample B.

[0059][the sample B which did not perform surface pure processing by TBCl, TMIn, and PH_3 by the second growth interface 104] C, O, and Si are detected by the second growth interface 104 as remains impurities, The concentration was made into area density, respectively, and was an equivalent for C:6.4x10 ^{10}atoms/cm^2, O:6.9x10 ^{11}atoms/cm^2, and Si:1.2x10 ^{12}atoms/cm^2. On the other hand, by the second growth interface 104, TBCl (19.4micromol/min), In the sample A which performed surface pure processing by TMIn (15.08micromol/min) and PH_3 (2.68 mmol/min), each remains impurities, such as C in the second growth interface 104, O, and Si, were below the detection limit. The minimum limit of detection in this measurement was an equivalent for C:6x10 ^{7}atoms/cm^2, O:6x10 ^{8}atoms/cm^2, and Si:6x10 ^{7}atoms/cm^2 here, respectively. Cl introduced as etching gas was not detected at all, either. The minimum limit of detection of Cl was a 3x10 ^{7}atoms/cm^2 grade here.

[0060]Although pure processing of the second growth interface 104 was mentioned as the example in this example and it explained it, this invention is also applicable to pure processing of the first growth interface 102.

[0061]In the second embodiment this example, this invention was applied to the InP system semiconductor laser element. In this example, after forming the semiconductor multilayer film which makes an active layer the top layer, the mask which covers a part of active-layer surface is formed, etching removes the portion of both the sides of this mask, and it provides MESASUTO ripe. Then, after wet etching removes a mask, pure processing which relates to this invention to the active-layer surface is carried out. After providing above-mentioned MESASUTO ripe, pure processing which relates to this invention also to the surface is carried out. Hereafter, this example is described with reference to drawing 10.

[0062]First, according to the usual crystal growth process, on the n type InP board 301, produce the double hetero structure which makes the InGaAsP/InGaAsP quantum well 307 an active layer, and SiO_2 is used as a mask, It formed MESASUTO ripe 310 with an about 2 micrometers deep width of 2 micrometers by dry etching. Then, after introducing this wafer in the MOVPE furnace and performing surface pure processing of above-mentioned this invention on the conditions same to the first re-growth interface 308 as the first embodiment, the p type InP layer 302, the n type InP layer 303, and the p type InP layer 304 were laminated one by one, and the current block structure was formed.

[0063]Next, after it takes out this wafer outside a MOVPE furnace and the usual wet etching process removes a SiO_2 mask, After supplying in the MOVPE furnace again and carrying out the above-mentioned surface pure processing of this invention under the same conditions as the first embodiment again to the second re-growth interface 309, the p type InP cladding layer 305 and the p-InGaAs contact layer 306 were formed. Then, the usual electrode formation process and the element separation process were performed, and the embedding type laser device was completed.

[0064]When the voltage-current characteristic of this element and the current-optical power characteristic are measured, compared with the conventional element which does not use surface pure processing of this invention, slope efficiency is improved sharply, and. The electric power-optical power conversion characteristic at the time of the Takamitsu output has been improved sharply, and it was checked that drive voltage required to obtain the same optical power is reduced sharply. When n type remains impurities, such as Si of the first re-growth interface 308 before current block layer formation, decreased in number by surface pure processing of this invention, [this] When leakage current decreased and n type remains impurities, such as Si of a clad and the second re-growth interface 309 before contact layer formation, decreased in number, a current barrier is removed and it is thought that it is what is depended on the effect to which drive voltage fell. In this example, although surface pure processing was performed to both the first re-growth interface 308 and the second re-growth interface 309, pure processing may be performed only to either 309, for example, the second re-growth interface.

[0065]In the third embodiment this example, except having changed the conditions of pure processing, semiconductor multilayer structure as well as the first embodiment was produced, and remains impurities densities, such as C in the second growth interface 104, O, and Si, were measured. The conditions of pure processing were shown in Table 1. Each item on the "processing conditions" of Table 1 is explained hereafter.

[0066](i) The kind t-butyl chloride (CH_3) $(_3CCl$:TBCl) of gas and bisdimethyl amino phosphine chloride ($[(CH_3)$ $_2]$ N_2PCl:BDMAPCl) were used.

(ii) The amount of supply of the gas into the flow MOVPE furnace of gas is shown.

(iii) The etching rate at the time of supplying only etching gas by the flow shown all over the etching-rate table is shown. This value is calculated by preliminary experiment.

(iv) The growth rate at the time of supplying only growth gas by the flow shown all over the growth rate table is shown. This value is calculated by preliminary experiment.

(v) The case where positive and layer thickness decreased the case where film thickness change index layer thickness increases was defined as negative, and the sum of a growth rate and an etching rate was defined as the "film thickness change index." It becomes an index of the layer thickness change before and behind a pure processing process.

(vi) A gas supply method continuation method is a method which supplies etching gas and growth gas to a definite-period-of-time continuation target. Intermittent methods are a definite period of time and a method supplied intermittently about etching gas and growth gas, and time to supply gas and time to stop supply of gas are repeated by turns.

(vii) When etching processing which used the etching solution before pure processing of the wet etching undoping InP layer 103 was performed, it was written as wet etching "it is."

[0067](Samples 1-4) As materials which have an etching operation, t-butyl chloride (CH_3) $(_3CCl$:TBCl) or bisdimethyl amino phosphine chloride ($[(CH_3)$ $_2]$ N_2PCl:BDMAPCl) is used, Trimethylindium (TMIn) and phosphine (PH_3) were used as crystal growth materials. After growing up 1.0 micrometer of undoping InP layers 103 as 1st growth layer by the decompression (60Torr) MOVPE method on the Sn dope {001} InP board 101 like drawing 1, a wafer is once taken out from a MOVPE furnace and air exposure is carried out for 12 hours. Then, wet etching of the surface of the undoping InP layer 103 was carried out with sulfuric acid content liquid, and it rinsed with pure water continuously.

[0068]Then, this wafer is again thrown in in a MOVPE furnace, and after performing pure processing on the conditions shown in Table 1, the 0.5-micrometer undoping InP layer 105 was re-grown up as 2nd growth layer.

[0069]The pure processing in each sample is as follows.

[0070]Pure processing was not performed by the sample 1.

[0071]In the sample 2, according to the second growth interface 104 in front of the 2nd growth

start, TBCl, TMIn, and PH_3 were supplied for 10 minutes on the surface of the wafer in the MOVPE furnace, and surface pure processing was performed. The amount of supply of each gas is as having been shown in Table 1. Supply of gas was taken as the continuation method. The substrate temperature at the time of pure processing was 625 **. Layer thickness change of the undoping InP layer 103 before and behind processing was not accepted.

[0072]In the sample 3, the second growth interface 104 in front of the 2nd growth start performed the following processings in the MOVPE furnace. That is, after supplying (i)TBCl, TMIn, and PH_3 for 1 minute on the surface of a wafer, for [(ii)] 15 seconds, the step of purging by supplying PH_3 in large quantities was repeated 20 times, and was carried out. The amount of supply of each gas is as having been shown in Table 1. The substrate temperature at the time of pure processing was 625 **. Layer thickness change of the undoping InP layer 103 before and behind processing was 100 nm or less.

[0073]In the sample 4, according to the second growth interface 104 in front of the 2nd growth start, bisdimethyl amino phosphine chloride (BDMAPCl), TMIn, and PH_3 were supplied for 10 minutes on the surface of the wafer in the MOVPE furnace, and surface pure processing was performed. The amount of supply of each gas is as having been shown in Table 1. Supply of gas was taken as the continuation method. The substrate temperature at the time of pure processing was 625 **. Layer thickness change of the undoping InP layer 103 before and behind processing was not accepted.

[0074](Samples 5-6) As materials which have an etching operation, t-butyl chloride (CH_3) $(_3CCl$:TBCl) or bisdimethyl amino phosphine chloride ($[(CH_3)\ _2]\ N_2PCl$:BDMAPCl) is used, Trimethylindium (TMIn) and phosphine (PH_3) were used as crystal growth materials. After growing up 1.0 micrometer of undoping InP layers 103 as 1st growth layer by the decompression (60Torr) MOVPE method on the Sn dope {001} InP board 101 like drawing 1, a wafer is once taken out from a MOVPE furnace and air exposure is carried out for 12 hours. Then, without performing wet etching, this wafer was again thrown in in the MOVPE furnace, and pure processing was performed on the conditions shown in Table 1. Then, the 0.5-micrometer undoping InP layer 105 was re-grown up as 2nd growth layer.

[0075]The pure processing in each sample is as follows.

[0076]Pure processing was not performed by the sample 5.

[0077]In the sample 6, according to the second growth interface 104 in front of the 2nd growth start, TBCl, TMIn, and PH_3 were supplied for 10 minutes on the surface of the wafer in the MOVPE furnace, and surface pure processing was performed. The amount of supply of each gas is as having been shown in Table 1. Supply of gas was taken as the continuation method. The substrate temperature at the time of pure processing was 625 **. Layer thickness change

of the undoping InP layer 103 before and behind processing was not accepted.

[0078]Each layer thickness change under pure processing of each above-mentioned sample was 100 nm or less. About each above-mentioned sample, the degree of remains impurities detailed was measured by SIMS like the first embodiment. A result is shown in Table 1 and drawing 2 - 7. Drawing 2 - 7 correspond to the measurement result of the samples 1-6, respectively. "n. d." means that it was not able to detect among Table 1. In sample NO.5, although the concentration corresponding to an applicable peak was computed, since distinction with a noise was difficult, the numerical value was shown as a reference value. By drawing 2 -7, the numerical value (vertical axis) calculated as impurity density (unit: atoms/cm^3) was converted as area density, and this value was made to correspond to an applicable peak, and was indicated all over the figure (unit: atoms/cm^2).

[0079]The following things became clear from the obtained result. That is, remains impure object surface density is notably reduced by adjusting the supply ratio of etching gas and growth gas so that a film thickness change index may be set to 6 nm or less (0.1nm/(sec) or less). Especially Si is removed effectively. A gas supply method has an effective intermittent type. Remains impurities density is notably reduced by considering it as intermittent supply. It is lower for remains impurities density not to carry out wet etching before pure processing.

[Table 1]

表1

試料			1	2	3	4	5	6
処理条件	エッチングガス	種類	なし	TBCL	TBCL	BDMAPCL	なし	TBCL
		流量（μmol/min）		19	38	27		19
		エッチング速度（nm/min）		20.5	36.8	14 4		20.5
	成長ガス	種類		TMIn	TMIn	TMIn		TMIn
		流量（μmol/min）		18	27	14		18
		成長速度（nm/min）		20.5	34.8	17.9		20.5
	膜厚変化指数（nm/min）			0	-4.2	3.5		0
	ガス供給方式			連続	間欠	連続		連続
	ウエットエッチング		有り	有り	有り	有り	なし	なし
評価結果	残留不純物面密度（atoms/cm^2）	Si	1.2E+12	2.5E+11	5.4E+10	5.4E+10	4.5E+11	N.D.(4.7E+9)
		C	5.0E+10	3.3E+10	N.D.	N.D.	N.D.	N.D.

[0080]In the fourth embodiment this example, a gas mass flow ratio is changed and the same experiment as the third embodiment is conducted.

[0081]In the same sample structure as drawing 1, [as surface pure processing conditions in the second growth interface 104] The amount of supply of TBCl which is etching gas 19.4micromol/min (the etching rate of InP is used and it is an equivalent for 20.5 nm/min), PH_3 amount of supply is made regularity with 2.68 mmol/min, the amount of supply of TMIn was changed between 0-30micromol/min, surface pure-for 10 minutes processing was performed, and the undoping InP layer 105 was grown up continuously. It investigated about the remains Si concentration of the 2nd interface by SIMS analysis continuously.

[0082]That (the "remains Si (continued type)" among a figure and display) to which drawing 8 changed the TMIn flow of the sample 2 in the third embodiment, and the thing (the "remains Si (intermittence type)" among a figure and display) to which the TMIn flow of the sample 3 in the third embodiment was changed are shown.
[0083]That to which drawing 9 changed the TMIn flow of the sample 4 in the third embodiment is shown.
[0084]The growth rate (namely, film thickness variation speed of the undoping InP layer 103 (the first semiconductor layer)) of InP and growth by TBCl and TMIn, and positive and etching were shown in drawing 8 and drawing 9 as negative with the area density of the remains Si.
[0085]When remains Si concentration decreased with the amount of supply of TMIn also in which system, and remains Si concentration showed the minimum in the neighborhood a growth rate becomes [sec] in 0nm /and also the TMIn flow was increased, remains Si concentration rose again. When this supplies only TBCl of etching gas to the second growth interface 104, the surface remains Si have a weak combination of Si-Cl compared with combination of Si-P, although 1 ** is desorbed from the surface as volatile chloride $SiCl_x$, and combination of Si-Cl goes out immediately -- again -- the surface -- the time -- adhering -- although. The stable III fellows site which Si occupied till then is buried with In, and it thinks because it is desorbed from the surface, without the ability of Si once desorbed from the surface to adhere to the InP surface again at the same time Si will be desorbed from the surface as $SiCl_x$, if TMIn is supplied simultaneously with TBCl. Therefore, the desorption efficiency of Si serves as the maximum in the hit where the etching rate of InP by TBCl and the growth rate of InP by TMIn balance exactly. Before Si ****s shortly, an InP layer grows, and if the growth rate of InP by TMIn exceeds the etching rate of InP by TBCl, since surface pure processing is no longer performed, it will be thought that the remains Si concentration in the second growth interface 104 rises.
[0086]From the result of drawing 8 and drawing 9, when it was considered as less than 0.1nm/sec layer thickness variation speed and there was no layer thickness change in particular substantially, it became clear that remains Si density was reduced notably.
[0087]As mentioned above, it is clear that this invention is not limited to each above-mentioned embodiment, but each embodiment may be suitably changed within the limits of technical idea of this invention although this invention was explained based on the embodiment.
[0088]For example, although TBCl and bisdimethyl amino phosphine chloride ($[(CH_3)_2] N_2 PCl$) were used in the above-mentioned embodiment as materials which have an etching operation, Other Cl system materials (HCl), for example, hydrogen chloride, chlorination methyls ($CH_3 Cl$), A carbon tetrachloride (CCl_4), bisdimethyl amino ARUSHIN chloride ($[(CH_3)_2] N_2AsCl$), phosphorus trichloride (PCl_3), 3 chlorination arsenic $AsCl_3$, chlorine (Cl_2), and

same Br system materials and I system -- materials and F system -- materials may be used. When using other materials, the decomposition efficiency and etching efficiency of materials change with materials, but. As fundamentally shown in the above-mentioned embodiment, the etching efficiency greatest by making the etching rate of the semiconductor layer by etching materials and the growth rate of the semiconductor layer by crystal growth materials balance is acquired, and the same effect is acquired.

[0089]Although the above-mentioned embodiment explained as an example the case where the MOVPE method was used as a crystal growth method, other growth techniques, for example, a molecular beam epitaxy (MBE) method and the gas source MBE (GSMBE) method, the organic metal MBE (MOMBE) method, the chemicals beam growing-up (CBE) method, etc. may be used. In the above-mentioned embodiment, although InP system material was explained, this invention is not restricted to this and can be applied to semiconducting materials, such as other III-V fellows compound semiconductors, such as GaAs, InAs, GaP, and GaN, and an II-VI fellows compound semiconductor.

[0090]Although it was considered as 625 ** in the above-mentioned embodiment about substrate temperature, If it is a temperature range, for example, InP, in which the usual crystal growth is possible, for 400 ** - about 700 **, What is necessary is just to be for 400 to 800 **, if it is GaAs, and change by the substrate temperature of the etching rate of the semiconductor layer by etching materials or the growth rate of the semiconductor layer by crystal growth materials is amended, the etching efficiency greatest because both make it balance is acquired, and there is same effect.

[0091]Although the first gas containing the etching nature substance which has an etching operation to a semiconductor layer, and the second gas containing crystal growth materials were simultaneously supplied to the semiconductor layer surface in the above-mentioned embodiment, it can also be considered as the method which supplies these by turns. In this case, it is desirable to perform the change of growth gas and etching gas quickly as etching is performed after growth of the thickness about a 1-3-atom layer advances since it will become difficult to realize sufficient cleanliness factor if growth of a semiconductor layer advances too much.

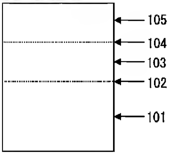
[0092]

[Effect of the Invention]Shape change is made into the minimum, without inducing the impurity diffusion in the semiconductor layer of a basis, and generating of a crystal defect according to this invention, as explained above, It is possible to remove stably the impurities contamination and the physical damage on the semiconductor substrate surface in front of crystal growth or the surface of a semiconductor before re-growth with sufficient reproducibility, and the performance improvement of a semiconductor device which has a growth interface has a big effect.

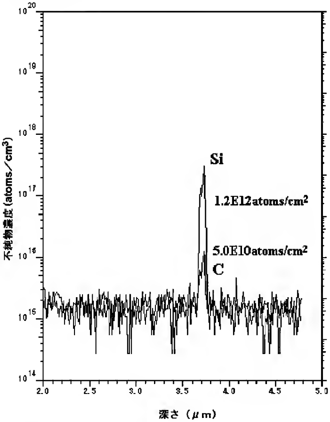
[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the structure of the semiconductor layer produced in the embodiment.
[Drawing 2]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 3]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 4]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 5]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 6]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 7]It is a figure showing the SIMS measurement result of the remains impurity density in an embodiment.
[Drawing 8]It is a figure showing the TMIn amount-of-supply dependence of the remains Si concentration in an embodiment.
[Drawing 9]It is a figure showing the TMIn amount-of-supply dependence of the remains Si concentration in an embodiment.
[Drawing 10]It is a figure showing the embedding type semiconductor laser structure in the second embodiment.
[Explanations of letters or numerals]
101 InP board
102 First growth interface
103 Undoping InP layer
104 Second growth interface
105 Undoping InP layer
301 N type InP board
302 P type InP layer
303 N type InP layer
304 P type InP layer
305 P type InP cladding layer
306 P-InGaAs contact layer
307 InGaAsP/InGaAsP quantum well

308 First re-growth interface
309 Second re-growth interface
310 MESASUTO ripe

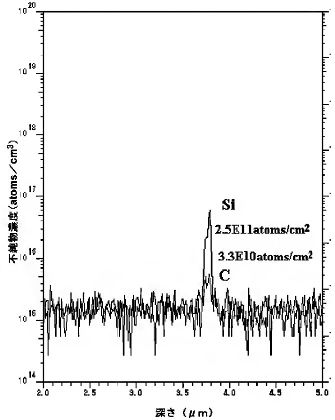
[Drawing 1]



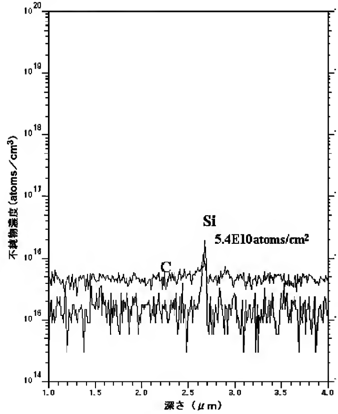
[Drawing 2]



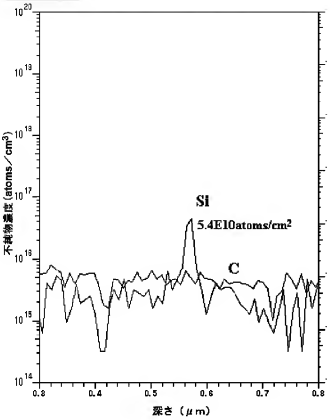
[Drawing 3]


Si
2.5E11atoms/cm2
3.3E10atoms/cm2
C
不純物濃度(atoms／cm3)
深さ（μm）

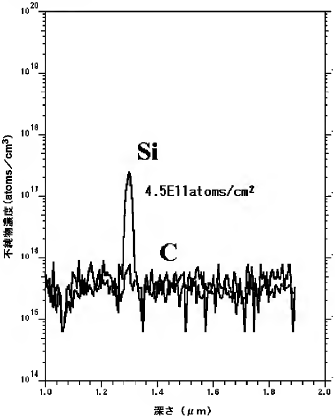
[Drawing 4]


Si
5.4E10atoms/cm2
C
不純物濃度(atoms／cm3)
深さ（μm）

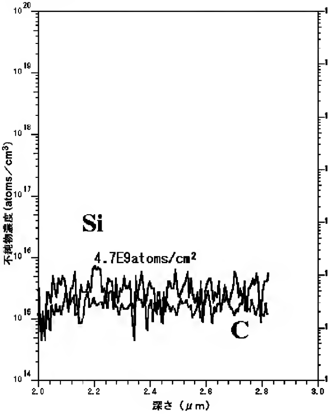
[Drawing 5]



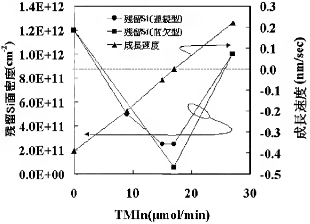
[Drawing 6]



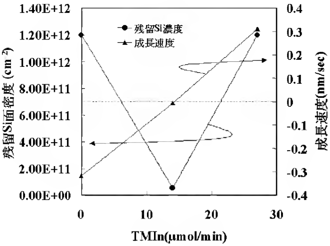
[Drawing 7]



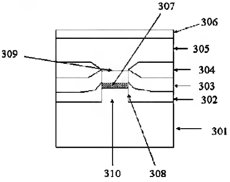
[Drawing 8]



[Drawing 9]



[Drawing 10]



[Translation done.]